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Technical evaluation

Testing of the lpGBT's EC-channel control link topologies

Abstract

This document is a report on the lpGBT's EC-channel control link testing. The EC-channel was designed for chip to chip communication. It was tested in various topologies by using several so-called VLDB+ (Versatile Link + Demo Boards). To test this feature different additional boards were used: the mHDMI-SMA and the mHDMI-mHDMI adaptor boards. In this report, a detailed description of the setup put in place, the performed tests and the obtained results will be given.

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Document History

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Contents

1 Introduction

The low-power Giga Bit Transceiver (lpGBT) is a radiation-tolerant ASIC designed to implement versatile high-speed bi-directional serial links in the experiments and environment of High Luminosity Large Hadron Collider (HL-LHC). The lpGBT is highly configurable and offers many useful features.

One of the features of the lpGBT is the EC-channel (Experiment Control channel) control link. The EC-channel is available to implement a control link between the lpGBT and other devices. It is commonly used to control one or several lpGBTs in the same bus. When controlling one lpGBT via another, the connection is called point-to-point. When several lpGBTs are controlled by a single master, the connection is then called multi-drop bus.

During the production testing of the lpGBT, just an emulation of the point-to-point communication could be tested. In this particular test, an FPGA emulates the behavior of an lpGBT being controlled by the tested lpGBT (the master) through EC. This test ensures that the EC-channel of every lpGBT was functional. However, this test could not validate all kinds of lpGBT-to-lpGBT communication modes as such a test would require a very complex and versatile testbench.

Several custom setups implementing various types of lpGBT to lpGBT(s) communication modes were put in place. The VLDB+ was chosen as a natural platform to perform this task together with a couple of custom boards that are shown below.

2 EC-channel point-to-point communication

The VLDB+ features a mHDMI connector which has the EDOUTECP/N and EDINECP/N differential pairs which constitute the EC-channel. This mHDMI connector was conceived to be able to communicate with the Slow Control ASIC (GBT-SCA) located on the former Versatile Link Demo Board or VLDB [1]. Two VLDB+ housing two different lpGBTs could also be interconnected through a their mHDMI connectors however, using mHDMI-SMA adaptors to properly map the EDOUTECP/N with the EDINECP/N pairs. In Figure 1 the mDHMI-SMA adaptor is shown.

Figure 1: mHDMI to SMA adaptor

This adaptor board is fully compatible with the VLDB+ mHDMI pinout and can take out the EDOUTECP/N and EDINECP/N signals through SMA connectors. This way, by using two of these boards we can properly swap the output with the input so two lpGBTs housed on two different VLDB+ can have a point-to-point communication. In Figure 2 a block diagram of such setup is shown.

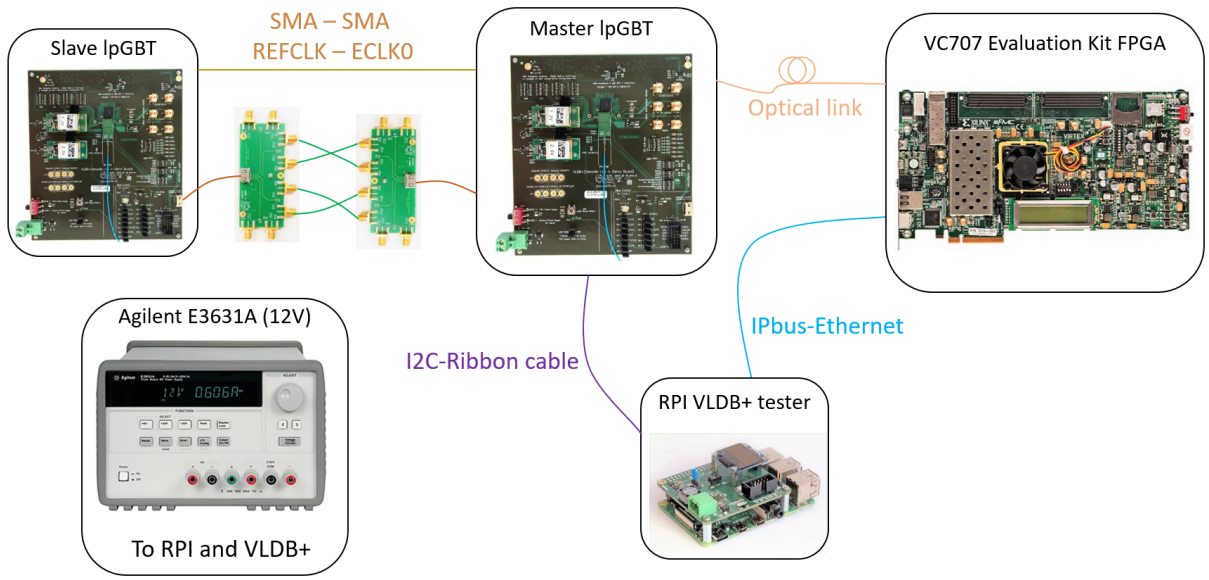

Figure 2: Block diagram of EC-channel point-to-point communication setup

One of the VLDB+ has its lpGBT in TRX Mode (Master) and the other in TX Mode (Slave). The lpGBT in TRX mode provides a reference clock of 40 MHz to the one in TX mode through SMA cables. At the same time, the VC707 FPGA runs the lpGBT-FPGA core [2] together with the GBT-SC core [3] in order to have both lpGBTs in Ready state and to be able to send commands through the EC channel. In Figure 3 the real setup is shown.

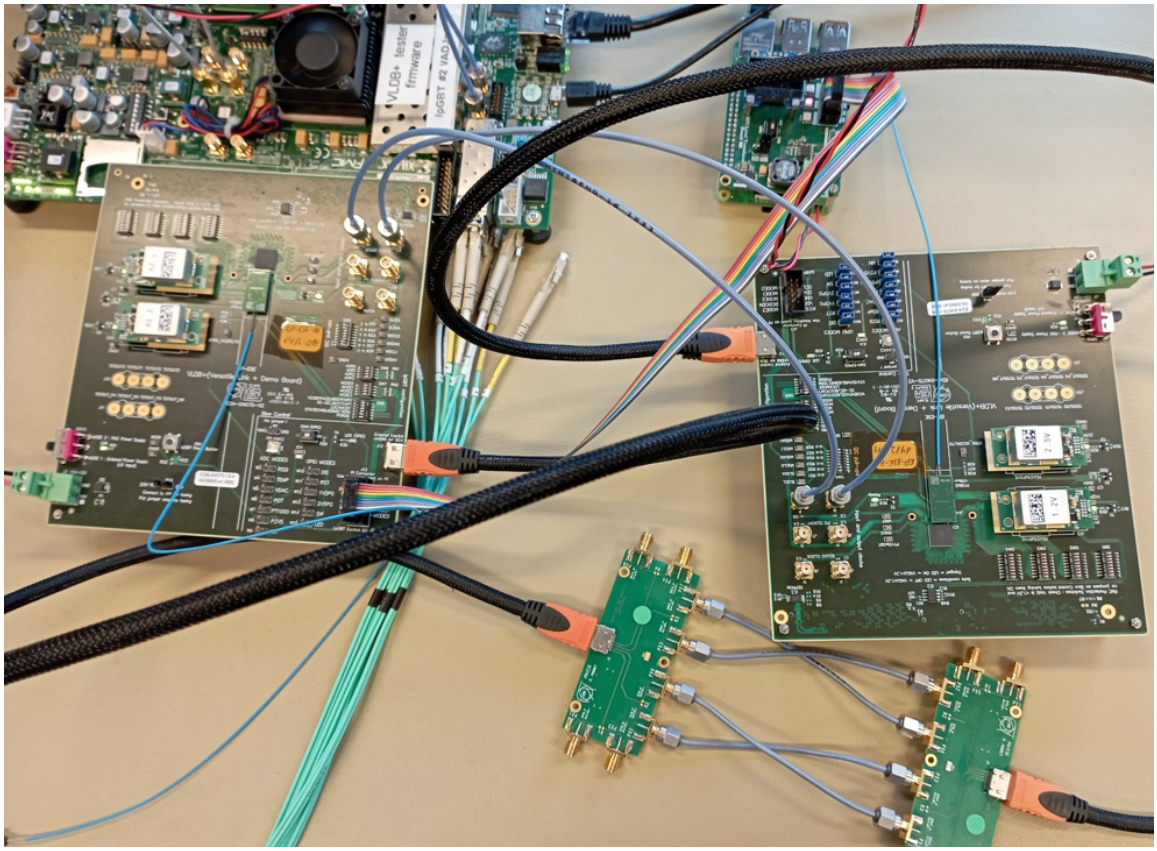

Figure 3: Setup to test the EC-channel point-to-point communication

The TRX (master) lpGBT configuration was the following:

- Mode TRX 10G FEC5, boot from ROM, reference-less locking, address 0x70;
- ROM configuration for TRX Mode;
- EDINEC enabled, termination enabled, no AC bias, no invert, pull-up enable and fixed phase;
- EDOUTEC enabled, tri-state disabled, drive strength set to 2.5 mA, no invert, no pre-emphasis;
- ECLK0 enabled, 40 MHz clock, drive strength set to 2.5 mA;
- DLL configuration done.

The TX (slave) lpGBT configuration was the following:

- Mode TX 10G FEC5, boot from ROM, external reference clock locking, EC termination enabled, address 0x71;
- ROM configuration for TX Mode;
- DLL configuration done (through EC).

After configuring the TRX lpGBT, the TX lpGBT receives a 40 MHz clock through its REFCLK pins. When this happens, the TX lpGBT reaches PAUSE_FOR_DLL_CONFIG_DONE state and it just needs to be programmed to reach the Ready state. To do so, the first EC command that is sent from the TRX lpGBT is writing the register [0x0fb] POWERUP2 with a value of 0x6 so DLL configuration is done. After this action, both lpGBTs are in Ready state.

From this point, thousands of write-read EC commands were continuously sent from TRX lpGBT to TX lpGBT to test the reliability of the link. Non-critical registers, which go from register 0x0 to register 0x1f, were written with random values (from 0x0 to 0xff) and read back through both I2C and EC. At the same time and after each EC write-read command, register [0x1e7] SCStatus was also read to check the parity result from the last command. The results show that no errors were observed when running this test continuously during several days. This is a good starting point since the length of the EC channel is longer than it could be on any board due to the mHDMI cables. In addition, the use of two adaptor boards were also having an impact on the signal integrity.

3 EC-channel multi-drop bus communication

With two TX lpGBTs

Despite the fact that a setup to test the EC-channel point-to-point communication was easy to establish using two VLDB+, the multi-drop bus topology was not straightforward. For this particular case, no mHDMI-SMA adaptor could be used. Therefore two specific mHDMI-mHDMI adaptor boards were manufactured for this particular test. One of the adaptor boards have the EDOUTEC and EDINEC swapped, the other does not. This way both boards can be used to interconnect more than 2 lpGBTs at the same time using several VLDB+. In Figure 4 two of these adaptors interconnected are shown.

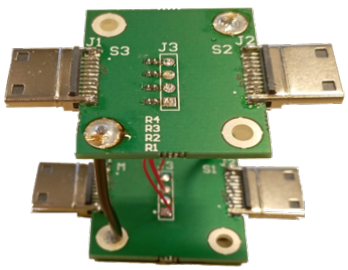

Figure 4: Two interconnected mHDMI to mHDMI adaptors

The four mHDMI connectors can be plugged into four different VLDB+ in order to have four lpGBTs on the same bus. The height between the two boards have to be adapted to match each VLDB+ connector. Because of this, the ground and signal connection was made with flexible cables. In Figure 5 the connection between the adaptor boards and three different VLDB+ is shown.

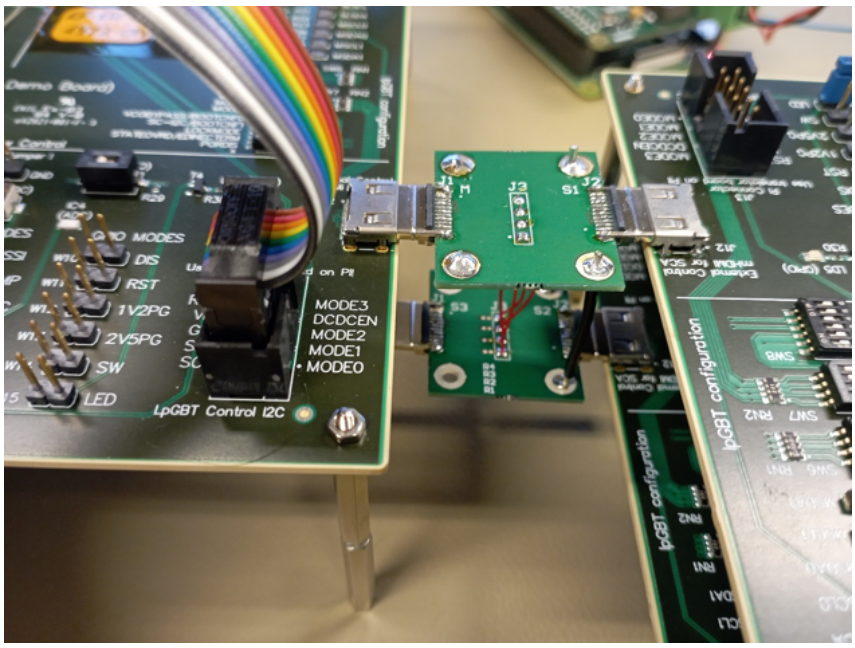

Figure 5: Adaptor boards plugged into three different VLDB+

Since this setup has two (slave) lpGBTs in TX mode, two reference clocks, ECLK0 and PSCLK1, are provided from the TRX (master) lpGBT to the TX lpGBTs.

The TRX (master) lpGBT configuration was the following (identical to the point-to-point test):

- Mode TRX 10G FEC5, boot from ROM, reference-less locking, address 0x70;
- ROM configuration for TRX;
- EDINEC enabled, termination enabled, no AC bias, no invert, pull-up enable and fixed phase;
- EDOUTEC enabled, tri-state disabled, drive strength set to 2.5 mA, no invert, no pre-emphasis;
- ECLK0 enabled, 40 MHz clock, drive strength set to 2.5 mA;
- PSCLK1 enabled, 40 MHz clock, drive strength set to 2.5 mA;
- DLL configuration done.

The configuration for the two TX lpGBTs were the following:

- Mode TX 10G FEC5, boot from ROM, external reference clock locking, EC termination enabled, addresses 0x71 and 0x72;
- ROM configuration for TX Mode;
- DLL configuration done (through EC).

The procedure is the same as for a point-to-point communication: after configuring the TRX lpGBT, both TX lpGBTs receive a 40 MHz clock through their REFCLK pins. Then both TX lpGBTs reach PAUSE_FOR_DLL_CONFIG_DONE state and the TRX lpGBT programs each of them through EC commands so that they reach Ready state.

In this case where two TX lpGBTs are used, the test procedure was slightly different: the same registers were written and read. Each time a TX lpGBT was addressed, new random values are generated. A good EC read response and an I2C validation with parity check is necessary to address the other TX lpGBT.

Once again, thousands of EC commands could be sent and received without issues. In this particular case, the length of the EC lines were shorter than for the point-to-point communication. However, the stubs between the TX lpGBTs and the EC bus which have a length of up to 170 mm, together with the non-ideal mHDMI to PCB connectivity, were having an impact on the signal integrity. Taking into account these deficiencies, the obtained results were outstanding. Typical PCB layouts housing lpGBTs on the same EC bus have stubs of a very reduced length with uniform tracks.

With three and more TX lpGBTs

The same hardware setup as Section 3 was used to be able to have an EC-channel multi-drop bus topology with three TX lpGBTs. However, to have five TX lpGBTs, a third mHDMI-mHDMI adaptor had to be added. In Figure 6 the setup of six different lpGBTs connected in the same EC bus is shown.

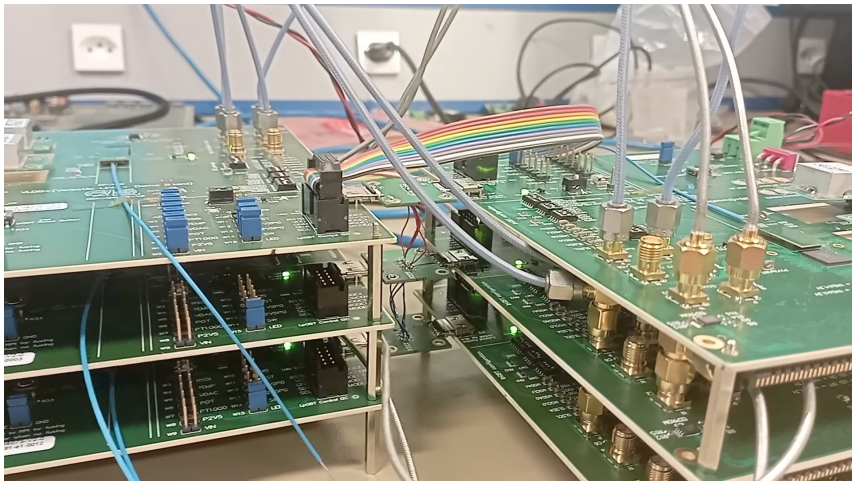

Figure 6: Adaptor boards plugged into six different VLDB+

In this case, the TRX lpGBT is not able to provide more than two reference clocks. Nevertheless, the two TX lpGBTs that receive the reference clock from the TRX are the ones providing reference clock to the three others. The configurations for TRX and TX lpGBTs are the same ones used for the setup in Section 3 except for the configuration of the ECLK0 and/or PSCLK1 to provide reference clocks to the remaining TX lpGBTs.

One more test that was added to this setup is the EC broadcast command: the TRX lpGBT sends the same command to all the TX lpGBTs. This is very useful to program several lpGBTs at the same time in case they have exactly the same configuration. This was tested by setting a value of 0 in the lpGBT address of the EC channel frame structure. Since the TX lpGBTs recognises the broadcast command, none of the lpGBTs reply to the command in order to avoid a collision. The broadcast command worked as well as the other commands and it was extensively tested. Finally, different track lengths were put in place to verify the operation of the continuous phase tracking of the EC channel. In order to do it, mHDMI-mHDMI connectors and cables were used for one specific VLDB+. The results showed that the lpGBT is able to adapt its input phase with respect to the incoming signal without issues.

4 Conclusions

The lpGBT features the so-called EC communication which allows the chip to send and receive specific commands that are used to configure and communicate with other devices.

In this report, EC communication tests on lpGBTs using two different EC topologies such as point-to-point bus and multi-drop bus were shown.

To test the first topology, two mHDMI-SMA adaptor boards were used together with two VLDB+. Both lpGBTs were booted from ROM to ease the configuration for two different modes of operation as TRX and TX. The results proved that this type of communication is functional and reliable.

To test the second topology, a mHDMI-mHDMI adaptor was manufactured. In this case, up to three adaptor boards were used together with six VLDB+, then, one TRX lpGBT and five TX lpGBTs were served by the same EC bus. The results proved that this type of communication as well as the broadcast commands are also functional and reliable.

Finally, different EC track lengths were tested to ensure that the continuous phase tracking mode was automatically tuning the phase aligner. The results showed that this feature also works well for the ePortRxEc.

References

[1] The Versatile Link Demonstrator Board

[2] The lpGBT-FPGA core

[3] The GBT-SC core