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Technical evaluation

Irradiation of the Versatile Link + Demo Board (VLDB+) with neutrons

Abstract

This document is a report on the irradiation with neutrons of the so-called VLDB+ (Versatile Link + Demo Board) for the evaluation of the different devices housed on it: the low-power Giga Bit Transceiver (lpGBT), the VTRx+ (Versatile Link + Transceiver), the bPOL12V DC/DC converter and the bPOL2V5 DC/DC converter. This board (and consequently the complete Versatile Link+ ecosystem) was irradiated with neutrons during operation to assess its performance as a system under radiations. The irradiation campaign took place at the *Université catholique de Louvain* (UCL) starting the 12^{th} of May 2022 and finishing the day after with a total irradiation time of 35 hours. During the following three weeks, the VLDB+ was also monitored in the so-called annealing process. In this report, a detailed description of the setup put in place, the tests performed and the obtained results will be given.

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Contents

1 Introduction

The **lpGBT**, **VTRx+** and **bPol** devices were designed at CERN in order to provide the next generation of electronic and opto-electronic components together with DC/DC converters for the HL-LHC detectors upgrades. The lpGBT and VTRx+ provide, among other things, a low-power link for bidirectional data transmission. On there side, the bPOL12V and bPOL2V5V convert a 12 V and 2.5 V input voltage to a 2.5 V and 1.2 V respectively to power devices such as the lpGBT and VTRx+. The four components, lpGBT, VTRx+, bPOL12V and bPOL2V5, were designed to withstand the harsh radiation environment typical of high energy physics experiments at HL-LHC. Despite the fact that individual radiation tests of such devices have been performed in order to ensure their proper operation, a radiation test where all these devices are operating together at the same time had never been carried out.

The **Versatile Link + Demonstrator Board** (VLDB+) was designed by the CERN EP-ESE team in order to have a board housing the lpGBT, VTRx+, bPOL12V and bPOL2V5 and made such a system-wide radiation test possible. The VLDB+ specifically prepared for radiation tests is showed in Figure 1.

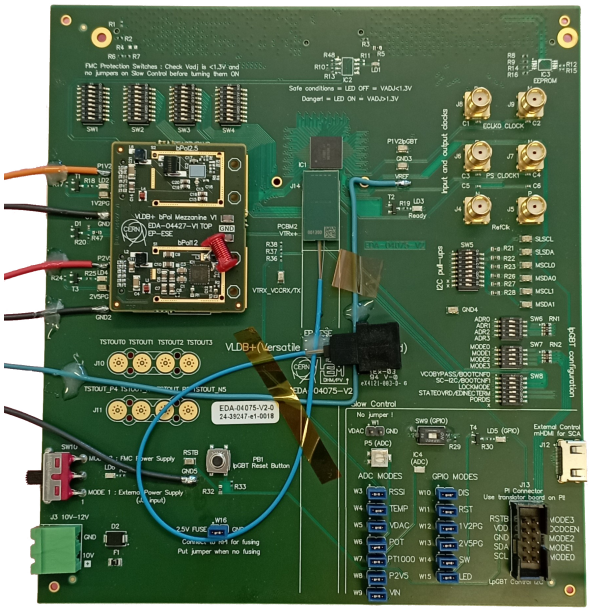

Figure 1: VLDB+ housing lpGBT, VTRx+ and bPOL Mezzanine

The bPol Mezzanine plugged on the VLDB+ and housing both bPOL12V and bPOL2V5V can be seen on the top left of the board. The lpGBT is located in the top middle of the board and below it, the VTRx+ with its blue fiber optic pigtail having a black MT-MPO adaptor at its end. The VTRx+ is in charge of the opto-electronic conversion of the serial stream transmitted and received by the lpGBT. The bPOL Mezzanine provides power to the whole board through the 10 V input: the bPOL12V transforms it into 2.5 V to power the bPOL2V5 and the VTRx+ receiver and the bPOL2V5 provides 1.2 V to power the lpGBT and the VTRx+ transmitter.

The lpGBT is controlled via I2C communication through the J13 black header located on the bottom right side of the board. Moreover, through this connector the RSTB (hardware reset) pin of the lpGBT and the Enable pin of both bPOL converters are available. The first one is used to perform resets to the chip and the second one to perform power cycles to the system by disabling and enabling both converters with one signal.

2 Results summary

A summary of the results from the VLDB+ irradiation are show in the table below:

During irradiation	
Test type	Results
VREF	A maximum drift of 3 mV drift was seen
ADC readings	No problems with ADC readings
Status registers	No wrong status
Downlink BERT	No errors
Uplink BERT	Sporadic errors due to non triplication of the lpGBT PRBS generator
Uplink FEC	Effective FEC against SEU
lpGBT and VTRx+ SEU	Effective SEU counters, unknown stuck of I2CM readings
bPOL12V and bPOL2V5	Stable bPOL output voltage (within ±8 %)

A summary of the results from the VLDB+ annealing are show in the table below:

During annealing	
Test type	Results
VREF	A maximum of 1.5 mV drift was seen
ADC readings	No problems with ADC readings
Status registers	Watchdog and Timeout triggered but the lpGBT was able to recover
Downlink BERT	No detected errors
Uplink BERT	No detected errors
Uplink FEC	No detected FEC
lpGBT and VTRx+ SEU	No detected SEU

More descriptive information of the front-end and back-end setups is provided in the chapters below, together with the results in plot format.

3 Front-end

Front-end area

The front-end area is a small room where the neutrons beam generator is located. In this room, the beam generator structure descends from the ceiling at an angle of 45 degrees and ends with the beam source which is pointing to a white platform where the electronics to be irradiated is installed. In Figure 2 the neutrons beam generator structure together with the electronics to be irradiated (bottom right corner) are shown. This picture was taken before the electronics was installed in front of the beam.

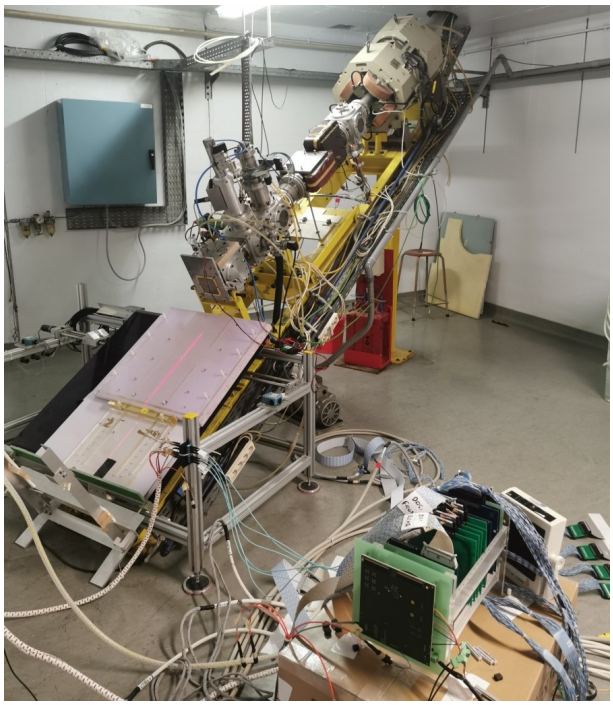

Figure 2: Front-end area

To ensure a good alignment with the beam, a laser pointer was used and can be seen as a red light on the white platform. The structure holding the electronics is described in the subsection 3. The radiation in this area before irradiation was around 2 μSv/h, a limited level allowing a safe installation of the electronics in the platform.

Most of the cables that went from the front-end electronics to the back-end electronics were around 10 meters long. The cables used to monitor and provide voltage in the VLDB+ were LEMO in order to reduce the noise as much as possible. The 10 meters Multi-Mode optical fibres used to interconnect the front-end to the back-end electronics were connectorized with Multi-Fibre Push On (MPO) to which was added an MPO to LC fanout of 1 meter.

The temperature in the front-end room before irradiation was around 26 ℃. Other physical characteristics as the humidity of the room were unknown.

Front-end setup

The VLDB+ was inserted in a mechanical structure hosting the other devices being irradiated by the team during this campaign (VCSELs, Silicon Photonics Chips, etc..). An extension of this structure was made to fit the VLDB+ and align its electronics (lpGBT, VTRx+ and bPOLs) to the neutrons beam. Figure 3 shows this electronics structure. The VLDB+ is on its left-hand side and the other devices are installed on the right-hand side (closer to the beam which is coming from right to left).

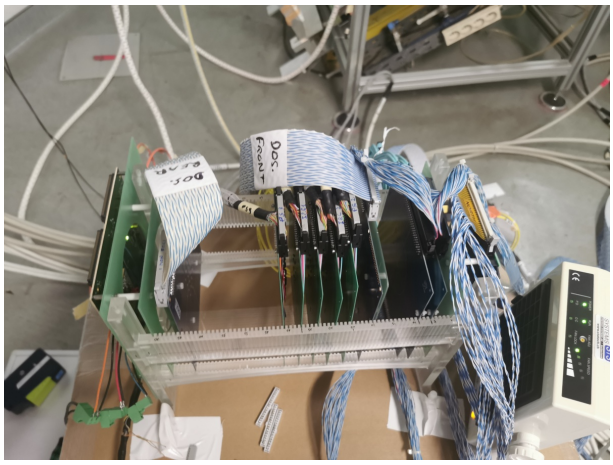

Figure 3: Electronics setup to be irradiated

As it can be observed on the left of Figure 1, three pairs of cables are going out from the VLDB+. These pairs of cables go to three different green header connectors. From top to bottom, the first pair was used to monitor the bPOL2V5 output (1.20 V), the second one to monitor the bPOL12V output (2.5 V) and the third one to monitor the lpGBT's Voltage Reference (VREF). These three headers can be seen in the bottom left of the Figure 3. A fourth header was used to provide 10 V to the VLDB+ board through the VLDB+ J3 connector located in the bottom left corner of the board.

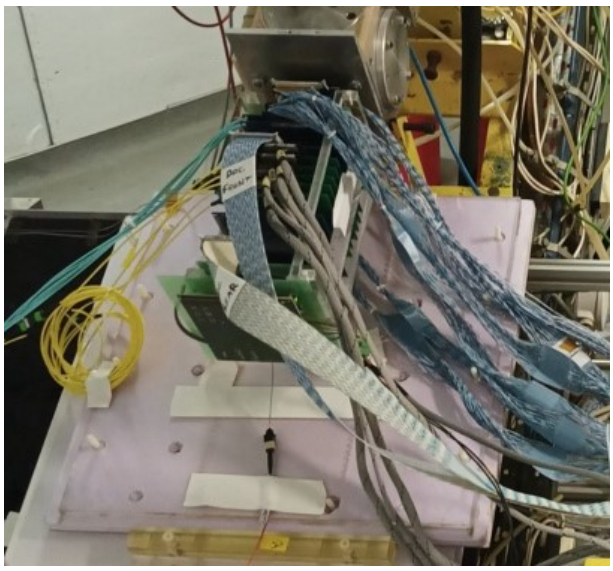

Figure 4: Front-end electronics final setup

In Figure 4 the placement of the structure holding all the electronics before their irradiation is shown. The devices are now facing the beam coming from the top of the picture. The VLDB+ is the board furthest from the source (40.1 cm).

Irradiation

As mentioned before, an extension of the front-end structure was made to fit the VLDB+. This extension was designed to align as best as possible the VLDB+ devices to the neutrons beam. Figure 5 shows a virtual representation of the VLDB+ depicting the representation of the beam (the white circle) hitting the VLDB+ taking into account its x,y position in the structure and its distance (40.1 cm) from the beam source (in the z direction). The distances of the four main devices from the beam center are also visible.

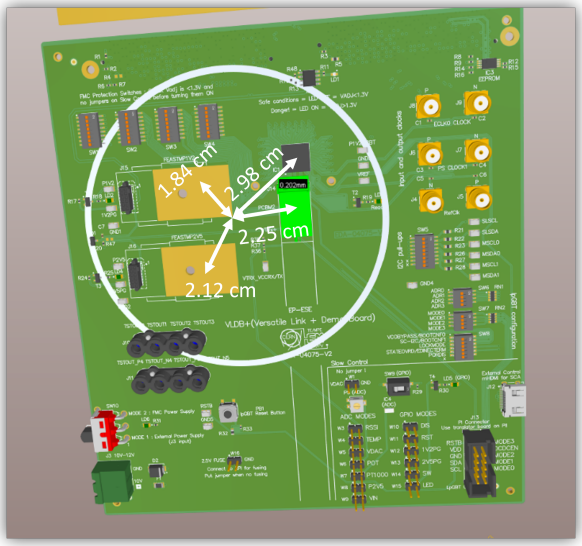

Figure 5: Virtual representation of the VLDB+ and the beam diameter (white)

These distances are necessary to calculate the fluence of the neutrons beam in each device. Taking into account the beam intensity at the distance of 40.1 cm from the source and the distance between the beam center in the VLDB+ and the different devices, the neutrons fluences during the corresponding 35 hours of irradiation could be calculated for each device after 35 hours of irradiation and are the following:

- lpGBT: 2.492×10^{14} n/cm^2
- VTRx+: 2.575×10^{14} n/cm^2
- bPOL12V: 2.603×10^{14} n/cm^2
- bPOL2V5: 2.686×10^{14} n/cm^2

These calculations were done by using the beam profile data at a distance of 39.5 cm presented in the thesis of Kim Bernier [1].

4 Back-end

Back-end area

The back-end area is located in the opposite room. The back-end and front-end rooms are separated by a blue door made of concrete. In addition, both rooms are also interconnected with holes of few tens of centimetres in order to pass the cabling through them. The electronic components that control and configure the VLDB+ were located in the back-end room together with the other equipment controlling the rest of the front-end electronics being irradiated during this campaign.

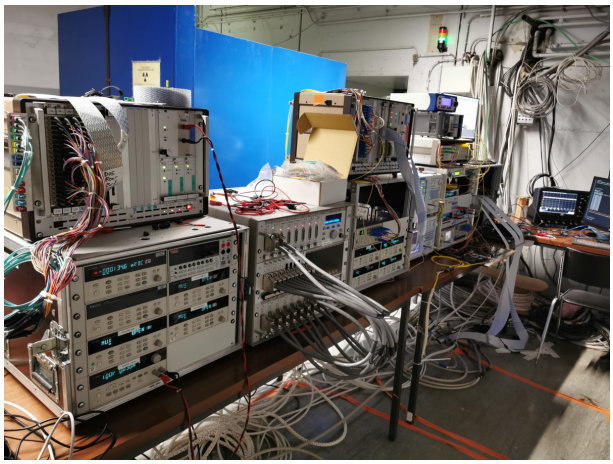

Figure 6: Back-end area

Figure 6 depicts the control setup located in the back-end area. The setup in charge of the VLDB+ was located on the right-hand side of the image, close to the black oscilloscope used to monitor the DC/DC output of the VLDB+.

Back-end setup

The back-end setup of the VLDB+ was made of two Lecroy WR104MXI scopes, one VC707 Evaluation Kit FPGA, one Keithley multimeter, one Raspberry Pi, one High-Precision Timing Board (HPTC) and one power supply. Part of this setup can be seen in Figure 7.

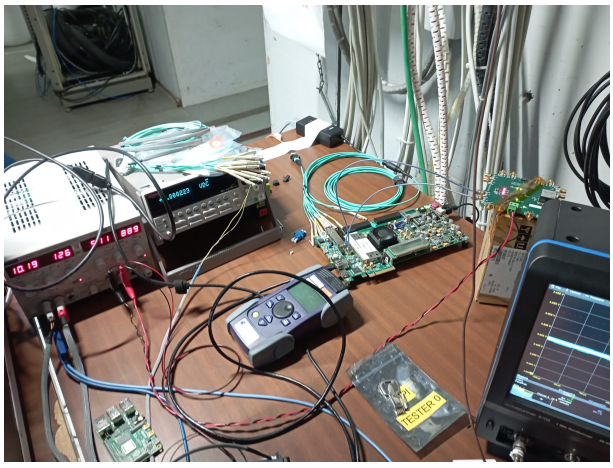

Figure 7: Back-end area

From left to right we can see the power supply providing power to both VLDB+ and HPTC boards, the Keithley multimeter, the VC707 Evaluation Kit FPGA, the HPTC and part of one of the Lecroy oscilloscopes.

The Raspberry Pi was the main element of the back-end setup. It was in charge of the configuration and monitoring of the Front-End electronics being irradiated (lpGBT, VTRx+, bPOLs) as well as the back-end side of the optical link represented by the VC707 evaluation kit. The two Lecroy oscilloscopes, however, were independent from the Raspberry PI control. One of them was connected to the bPOL12V output and the other to the bPOL2V5 output. Both oscilloscopes were configured with a window trigger: anytime that the 2.5 V or the 1.2 V would left this window, it would trigger the oscilloscope. The window was set to 8 % of the nominal voltage value. This corresponds to a margin of 2.4426 V - 2.8674 V for the bPOL12V (nominal value of 2.655 V) and of 1.0994 V - 1.2906 V for the bPOL2V5V (nominal value of 1.195 V). The monitoring of the bPOL outputs was done during irradiation only.

If a trigger occurs, the oscilloscope would automatically save a screenshot and a file with the corresponding voltage data.

During the operation of the back-end setup without irradiation, the attenuation margins of both uplink (from the lpGBT to the back-end FPGA) and downlink (from the back-end FPGA to the lpGBT) paths was determined. The optical attenuation to start having errors in both downlink and uplink was around 16 dB.

Software

The Raspberry Pi 4B was running the whole software based in Python. It was communicating with the FPGA Evaluation Kit through Ethernet thanks to the IPBus firmware and software suite, with the Multimeter through GPIB communication and with the lpGBT through I2C communication.

The software was running two tests in parallel. These tests were the lpGBT Downlink and Uplink BERT (Bit Error Rate Test). While executing these two tests, other were executed just once, these are:

- lpGBT and VTRx+ status check
- System status registers check
- lpGBT's analog readings
- VTRx+ and lpGBT SEU readings
- lpGBT's VREF reading

This sequence was looped back infinitely and the duration of one cycle was defined by the duration of the downlink and uplink BER tests. The default cycle time was set to 52 seconds (as a trade-off between BERT precision and regularity of the registers checks) but other cycle times were used (3.4 s, 13 s, ...).
A description of the test scripts are described below:

- **lpGBT Downlink BERT**: The Evaluation Kit FPGA continuously sends PRBS7 data encoded in the lpGBT frame through the downlink optical path. The data is received by the VTRx+ and the lpGBT and verified through its downlink pattern checker. The pattern checker provides an error count that is read by the Raspberry every time a test cycle is completed.
- **lpGBT Uplink BERT**: The Evaluation Kit FPGA continuously receives PRBS7 data encoded in the lpGBT frame and transmitted by the VTRx+ through the uplink optical path. The PRBS pattern checker in the FPGA firmware provides an error count that is read by the Raspberry every time a test cycle was completed.
- **lpGBT and system status registers check**: The Raspberry also reads several status registers of the lpGBT as the *PLL/DLL Watchdog*, *PLL/DLL Timeout*, *ePortRx channels Timeout*, *Frame-Aligner state*, *Frame-Aligner not header count*, *Frame-Aligner loss of lock count*, *power-up state machine* and *brownout detector* flag.
- **lpGBT's analog readings**: The lpGBT performs several ADC conversions to read its internal temperature sensor, the bPOL2V5 output, the VTRx+ RSSI and the VLDB+ PT1000.
- **VTRx+ and lpGBT SEU readings**: The lpGBT performs I2CMaster commands to be able to communicate with the VTRx+ so the SEU counter could be read. The Raspberry checks the lpGBT's internal SEU counter.

- **lpGBT's VREF reading**: The Raspberry performs GPIB commands to measure the lpGBT's VREF by means of an external multimeter.

In addition to all the described tests, a feature was in charge of re-initialising the system in case the lpGBT lost the lock. In case that the lpGBT would lose the lock, the software would reset the chip, reconfigure it, calibrate its VREF and restart the tests.
Finally, during one particular run, power cycles of the VLDB+ was added to the cycle in order to see any unexpected behavior. The software was doing the same cycle procedure except that after each end of cycle, the system was shut-down during 2 seconds and powered-up for the next cycle. This test was done after 33 hours and 6 minutes after irradiation for around 50 cycles.

5 Setup summary

Block diagram

A block diagram of the full setup can be seen in Figure 8. In addition to what is shown in the block diagram, the power supply that was used to power the VLDB+ and the HPTC is the PL303QMD-P. On the other hand, the Raspberry Pi was powered through an independent power supply.

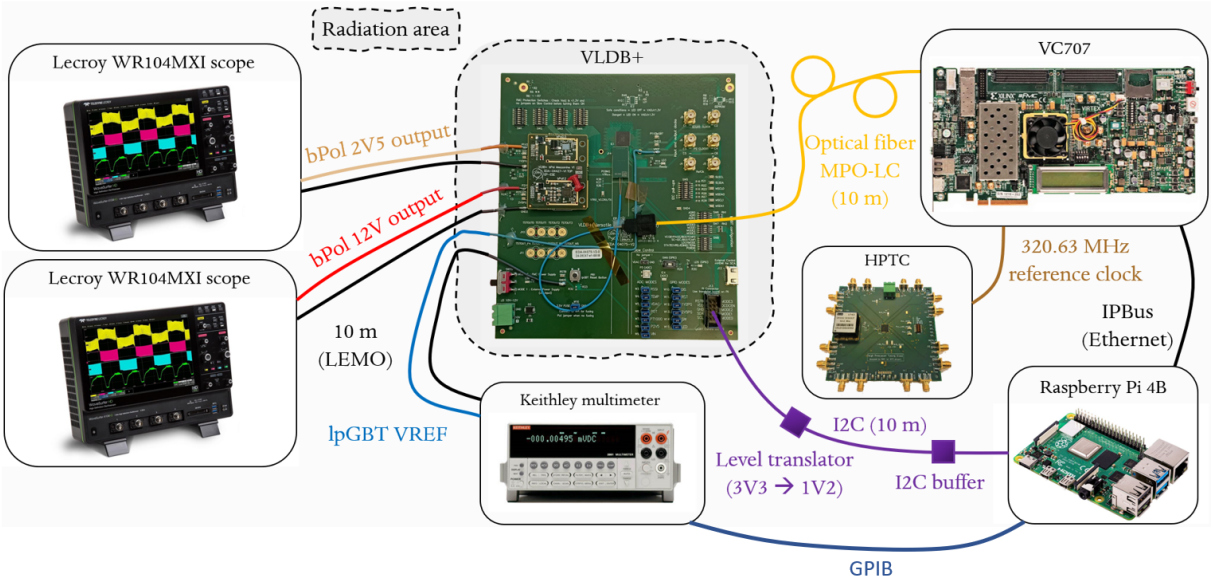

Figure 8: Setup block diagram

6 Results

The upcoming sections present the evolution of each monitored parameter, first during the 35 hours of irradiation, and then during the 500 hours of annealing at ambient temperature.

During 35 hours of irradiation

During the 35 hours of irradiation, the tester was stopped and restarted 6 specific times:

- 8h 30mn after start: VTRx+ SEU reading from the lpGBT I2CMaster test was added.
- 12h 48mn after start: more EPRx debugging was added.
- 23h 21mn after start: BER duration was decreased from 54 s to 3.4 s.
- 31h 10mn after start: BER duration was increased from 3.4 s to 14 mn.
- 33h 6mn after start: Power-down and power-up in every cycle with 54s BER.
- 33h 50mn after start: BER time was increased from 54s to 3.5 mn for annealing.

After each of these stops, the software was restarted. This caused dead times in the data taking during the irradiation which can be seen in the following plots.

lpGBT VREF

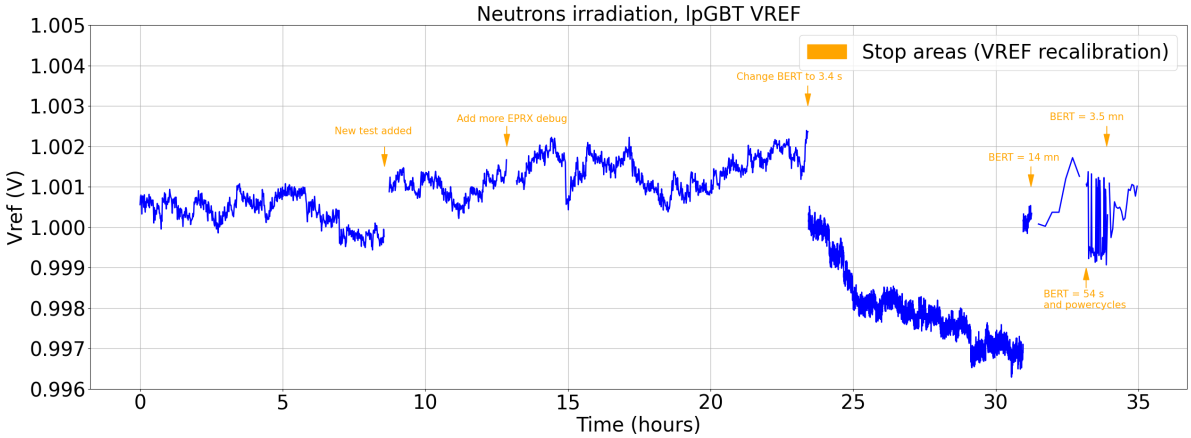

Figure 9: VREF during irradiation

Just before the irradiation, the lpGBT's VREF was calibrated to be as close as possible to 1 V. During the 35 hours of irradiation, there were 6 specific moments where the VREF control register was re-calibrated, explaining the jumps of the voltage reference value. The re-calibration software tries to find the best code for a VREF value with an error of 1 mV at maximum. In some cases, as in the first re-calibration, the VREF value worsens after re-calibration since it stops searching for the best code as soon as it gets a value with an error of less than 1 mV. Between the periods of time where the system was not restarted, the VREF remained stable around 1 V. The only period of time where a significant voltage decrease of 3 mV occurred was between 23h 21mn and 31h 10mn.
It is important to mention that the VREF generated by the lpGBT is used internally by the chip for its ADC and DAC IPs. Therefore, any variation of the VREF is expected to impact their performance.

lpGBT ADC readings

During irradiation different ADC readings were performed:

- The lpGBT's internal temperature sensor was read through its ADC;
- The VLDB+ PT1000 was driven by the lpGBT's current DAC so a voltage drop could be read through its ADC and the temperature variations could be monitored;
- The VTRx+ RSSI was also monitored by the ADC. To obtain the photodiode current from the lpGBT's ADC, the values from the voltage divider and from the bPOL2V5 output were used;
- The bPOL2V5 output was measured with the ADC by using a voltage divider that adjusts the voltage to be lpGBT compatible.

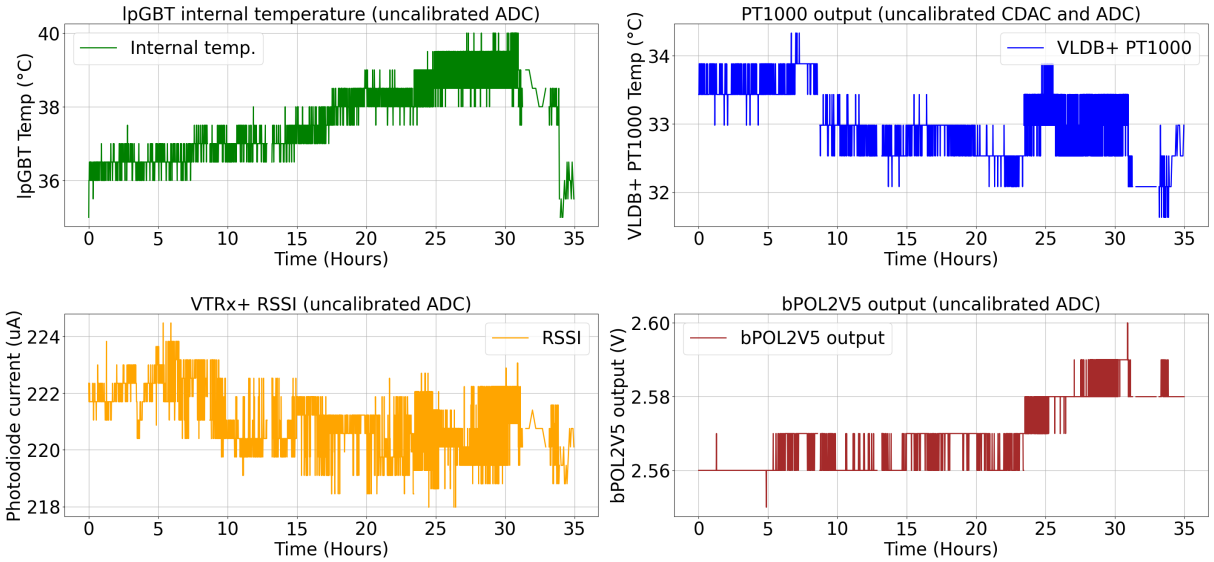

Figure 10: Performed lpGBT ADC readings during irradiation

In Figure 10, the reading of the four ADCs during irradiation is shown. Since the internal temperature monitor, ADC and CDAC of the lpGBT under test was not calibrated before irradiation, the temperature, current and voltage values that are shown have a non-negligible error. Since this error can be reduced by using calibration values, the main goal of this test was to ensure the operation of the ADC and CDAC features rather than the precision of the obtained values.

It can be seen that during the 35 hours of irradiation, the ADC values could be read without interruption. The ADC and CDAC features did not suffer from SEU and no drastic value changes that could not be explained by VREF re-calibration drifts or sudden temperature changes (due to power cycles) could be seen.

lpGBT status registers

During irradiation, none of the following status registers triggered:

- Watchdog PLL
- Watchdog DLL
- Timeout PLL
- Timeout DLL
- eLink Timeout
- Frame Aligner PUSM different than ”Track header”
- Frame Aligner with no header
- Frame Aligner loss of lock
- lpGBT PUSM different than Ready

This means that:

- if some of these registers were suffering from SEU, the TMR implemented in the lpGBT protected them efficiently
- the lpGBT Downlink and Uplink were locked during all the irradiation without any interruption.

lpGBT Downlink BERT

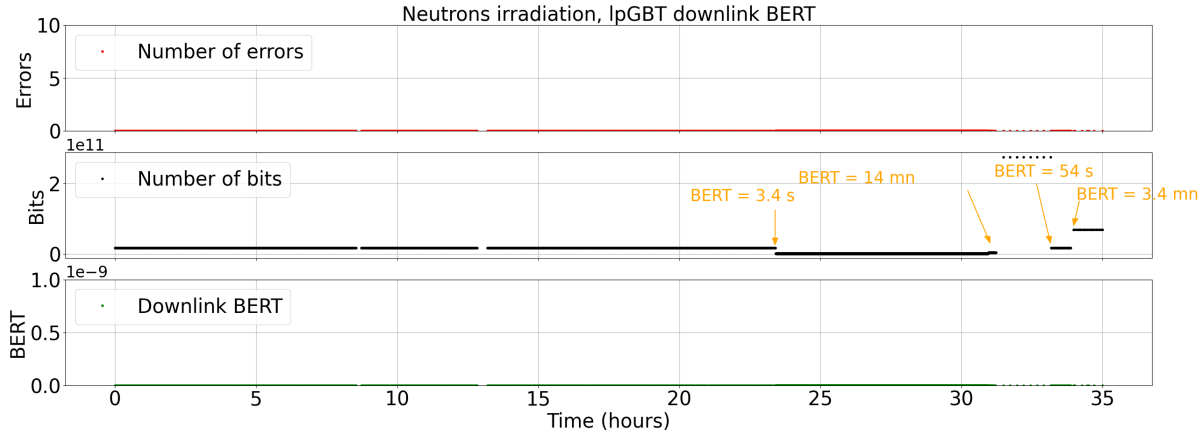

Figure 11: lpGBT Downlink BERT during irradiation

During irradiation, the BERT duration changed in different moments of the test to have more statistics. In Figure 11, 3 different plots are shown: number of errors, number of bits and BER (errors/bits). As it can be seen, not a single downlink error was detected during all the irradiation (except for some burst errors explained in Section 7)
During irradiation, the BERT duration changed:

- From start until 23h 21mn: 54 seconds
- From 23h 23mn until 31h 10mn: 3.4 seconds
- From 31h 12mn until 33h 6mn: 14 minutes
- From 33h 11mn until 33h 50mn: 54 seconds
- From 33h 55m until 35h: 3.4 minutes

lpGBT Downlink FEC

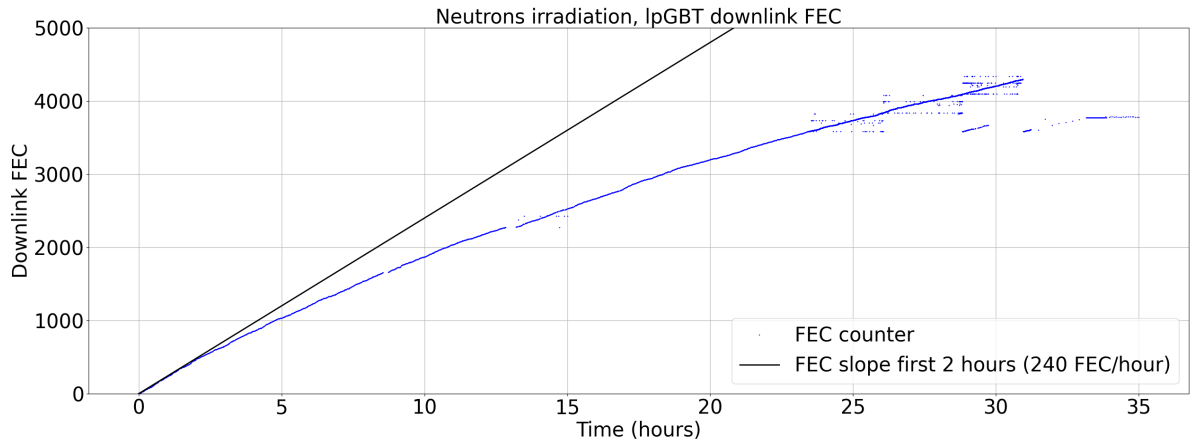

Figure 12: lpGBT Downlink FEC during irradiation

During irradiation, the downlink Forward Error Correction (FEC) was constantly increasing and protecting the downlink receiver against errors. In Figure 12 the downlink FEC during irradiation can be seen. A black line shows the FEC slope during the first 2 hours of irradiation. This visual help shows that the FEC slope decreased during irradiation: the FEC slope was decreasing at a rate of around 100 FEC/hour.

The most plausible explanation for this behavior is that the photodiode acts as a particle detector. As it degrades over time when being irradiated, it becomes less sensitive to neutrons. Nevertheless, since the optical data has a low attenuation the photodiode still detects it and does not lose performance.

In the plot it can be also seen that the FEC counter between hour 23 and 33 was showing values that were not following the curve. This was due to software problems that are explained in Section 7.

lpGBT Uplink BERT

During irradiation, the BERT duration changed in different moments of the test to have more statistics. In Figure 13, 3 different plots are shown: number of errors, number of bits and BER (errors/bits). Since the uplink data PRBS pattern generator was not designed to be protected against SEU, some sporadic uplink errors were detected during the irradiation. Moreover, between hours 31 and 33 where the BERT duration changed from 3.4 seconds to 14 minutes, it can be seen that the number of uplink bits do not correspond to a longer BERT time. This was due to an unexpected overflow on the firmware that caused to have no uplink errors.

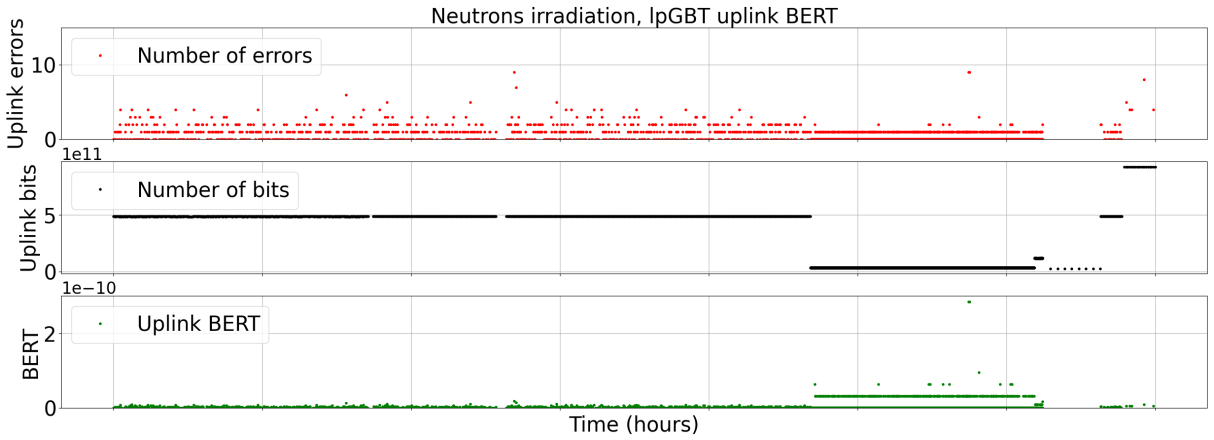

Figure 13: lpGBT Uplink BERT during irradiation

lpGBT Uplink FEC

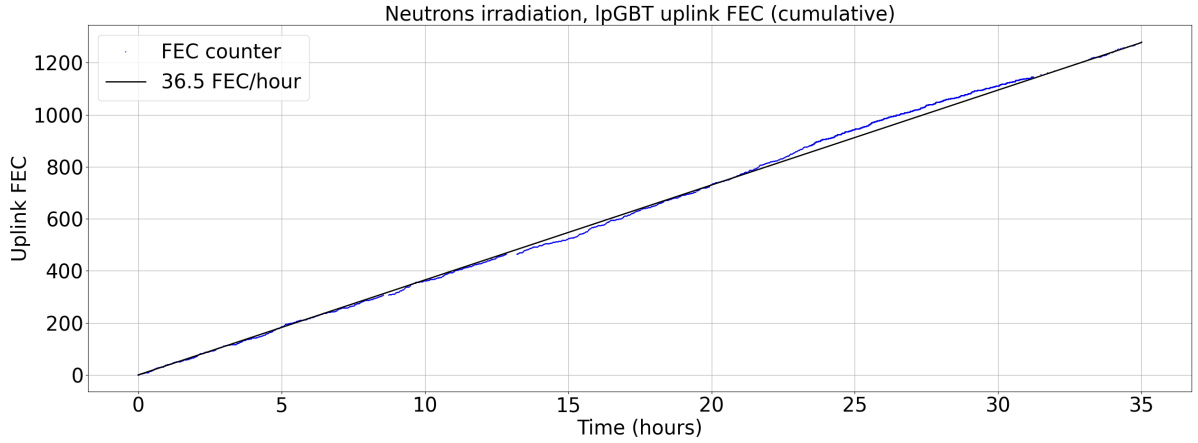

Figure 14: lpGBT Uplink FEC during irradiation

During irradiation, the uplink Forward Error Correction (FEC) was constantly increasing and protecting the uplink receiver against errors. In Figure 14 the uplink FEC during irradiation can be seen. A black line shows the FEC slope during the whole irradiation. This visual help shows that the FEC had its ups and downs but remained almost linear during the 35 hours. When looking at Section 6 further down, it can be seen that the neutrons flux was increasing and decreasing in the same way as the uplink FEC.

lpGBT and VTRx+ SEU

The SEU counter was monitored in both lpGBT and VTRx+ devices. The lpGBT SEU counter was read from its internal registers and the VTRx+ SEU counter from its own by using the I2CMaster of the lpGBT. In Figure 15 the VTRx+ and lpGBT SEU counters can be seen. The VTRx+ SEU counter was not read during the first 8.5 hours of irradiation. Then, it was read during the rest of the irradiation. The lpGBT SEU counter was read from the beginning. As it can be seen, the various resets performed in the lpGBT was making its SEU counter to reset but not the one from the VTRx+. For the lpGBT, the SEU counter slope was more or less constant with a value of around 800 SEU/hour. For the VTRx+, this value is around 100 SEU/hour. It can also be seen that the VTRx+ SEU counter stopped counting for around 3 hours. These constant SEU values were actually read from the I2CMaster of the lpGBT. There is no explanation for this behavior. Nevertheless

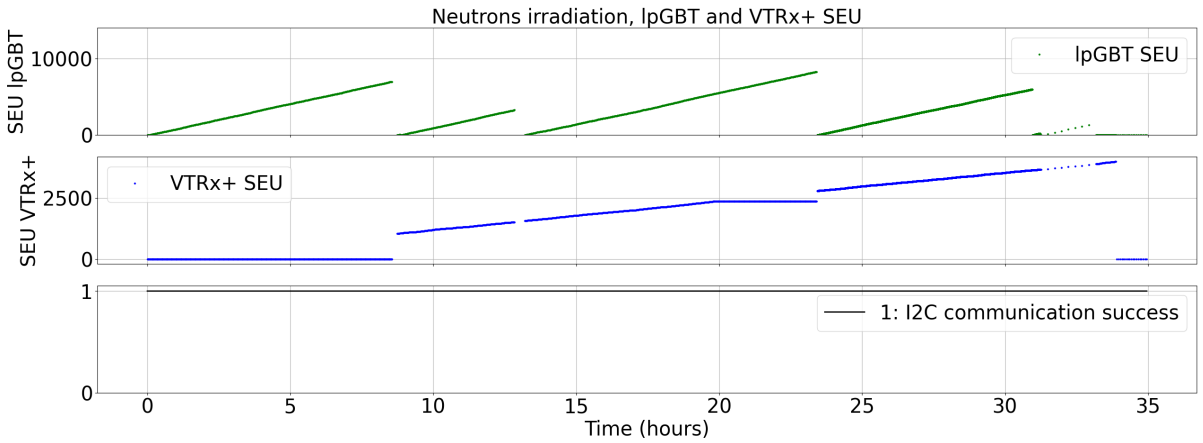

Figure 15: lpGBT Uplink FEC during irradiation

an lpGBT reset was enough to make the VTRx+ SEU counter work again. In case the I2CMaster of the lpGBT was the issue, an independent I2CMaster reset would probably also fix this issue.

Deuteron current

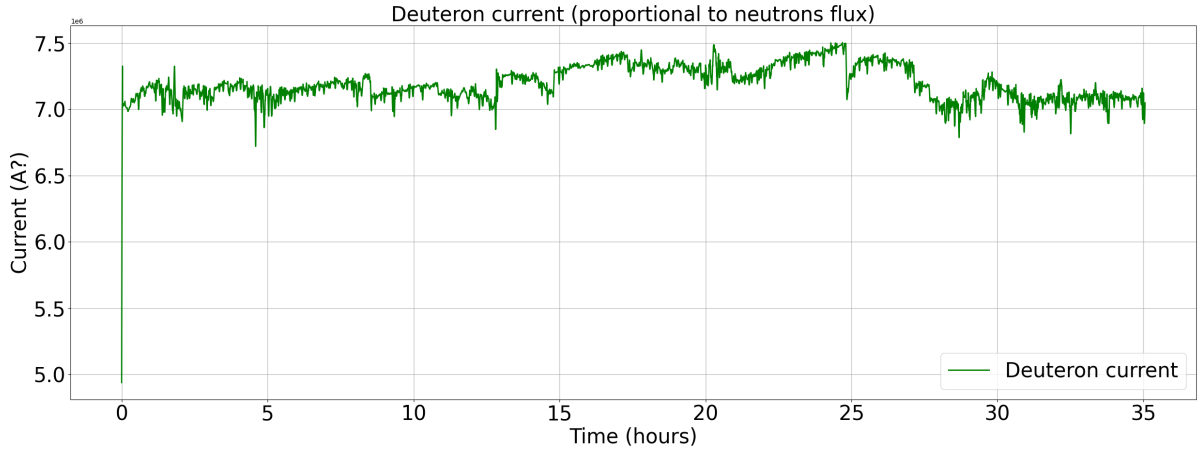

Figure 16: lpGBT Uplink FEC during irradiation

The deuteron current is a technique used to estimate the neutron flux in an irradiated system. The deuteron current is measured by the number of deuterons flowing into a specific particle detector per unit time and it is proportional to the neutron flux because the number of deuterons generated is directly related to the number of neutrons interacting with deuterium nuclei. In Figure 16 the deuteron current during the 35 hours of irradiation can be seen. This plot was previously filtered to remove the excessive noise that was screening out useful values. The neutrons flux was more or less constant during all the irradiation. There were small up and downs of the flux that can be linked to an increase and decrease of SEU and FEC. For instance, between hour 21 and 25, the uplink FEC counter slope slightly increased and this can be associated to a higher neutrons flux that can be seen in the deuteron current increase between the same hours.

bPOL12V and bPOL2V5 outputs

During irradiation both bPOL12V and bPOL2V5 outputs were monitored and the scopes were triggering when these values were exceeding the ±8 % margin. During irradiation, both bPOLs did not have any suspicious voltage output that could be originated by the neutrons irradiation. In Figure 17 and Figure 18 an automatic screenshot of their outputs when performing power cycles tests on the system can be seen. The power cycles ensured, among other things, that the oscilloscopes were still properly configured at the end of the irradiation. Due to the small voltage and time scales set to capture possible spikes, just a small fraction of the voltage drop can be seen.

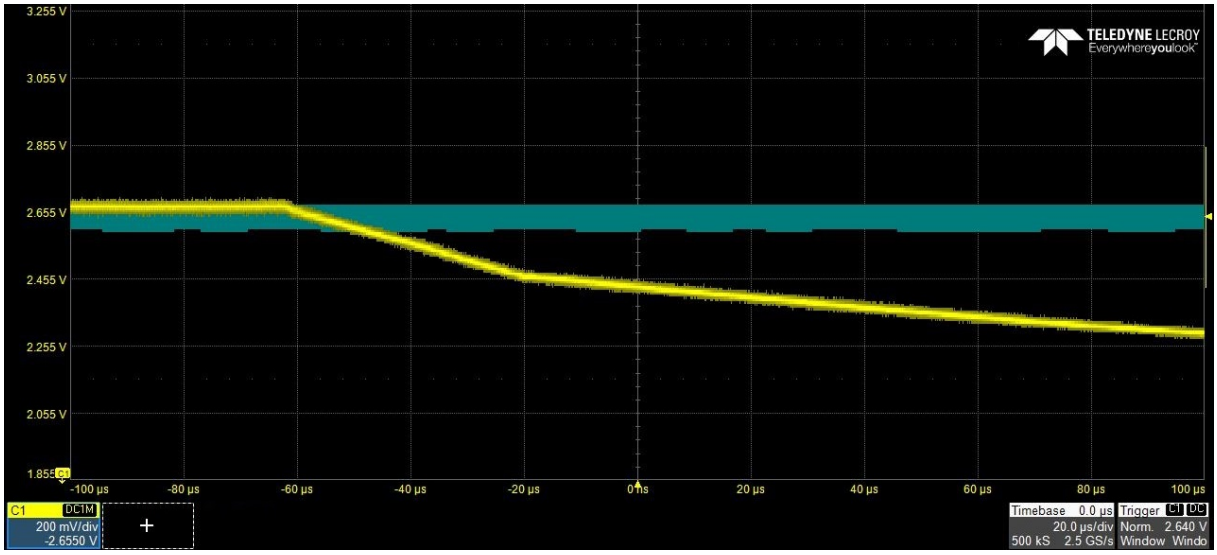

Figure 17: bPOL12V output during VLDB+ power cycle

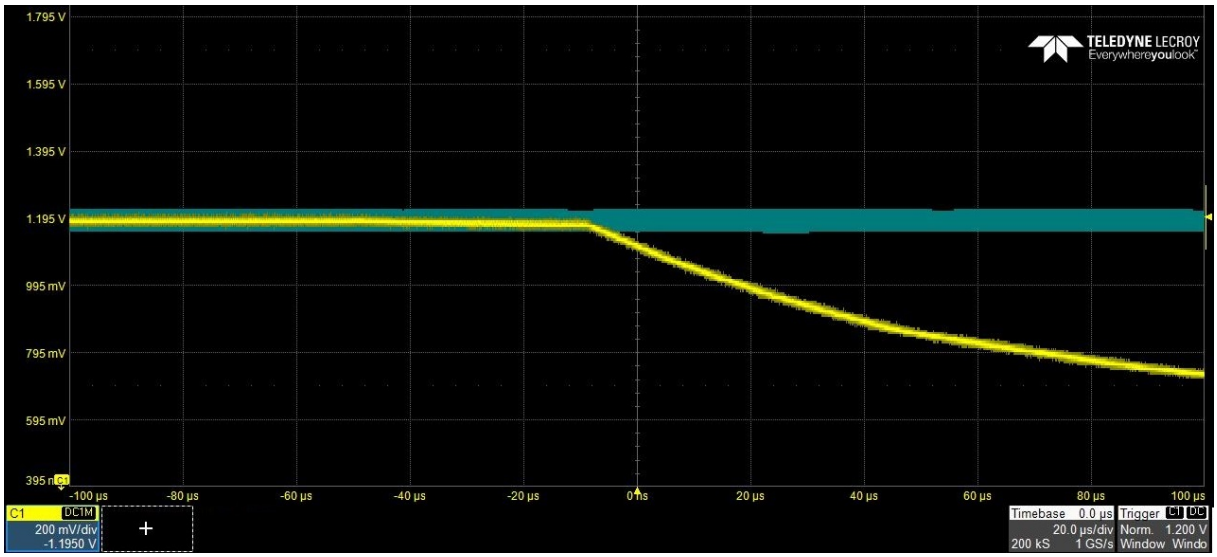

Figure 18: bPOL2V5 output during VLDB+ power cycle

During 500 hours of annealing

During the 500 hours of annealing, the tester was never stopped. However, a few events happened:

- 102 hours after beam stop: Communication with RPI was lost.
- 120 hours after beam stop: Communication with RPI was re-established.
- 456 hours after beam stop: Re-initialisation procedure was automatically triggered.

lpGBT VREF

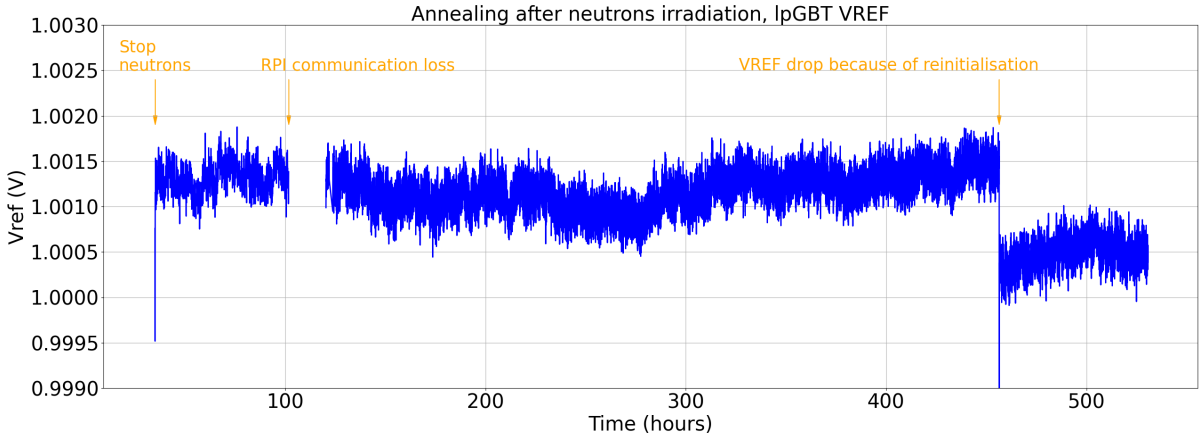

Figure 19: VREF during annealing

In Figure 19 the VREF during the annealing can be seen. The Voltage Reference remained stable around 1.0013 V. The only remarkable shift was caused by the re-initialisation of the lpGBT which made the VREF to be re-calibrated to a value closer to 1 V.

lpGBT ADC readings

The different ADC readings were also performed during annealing.

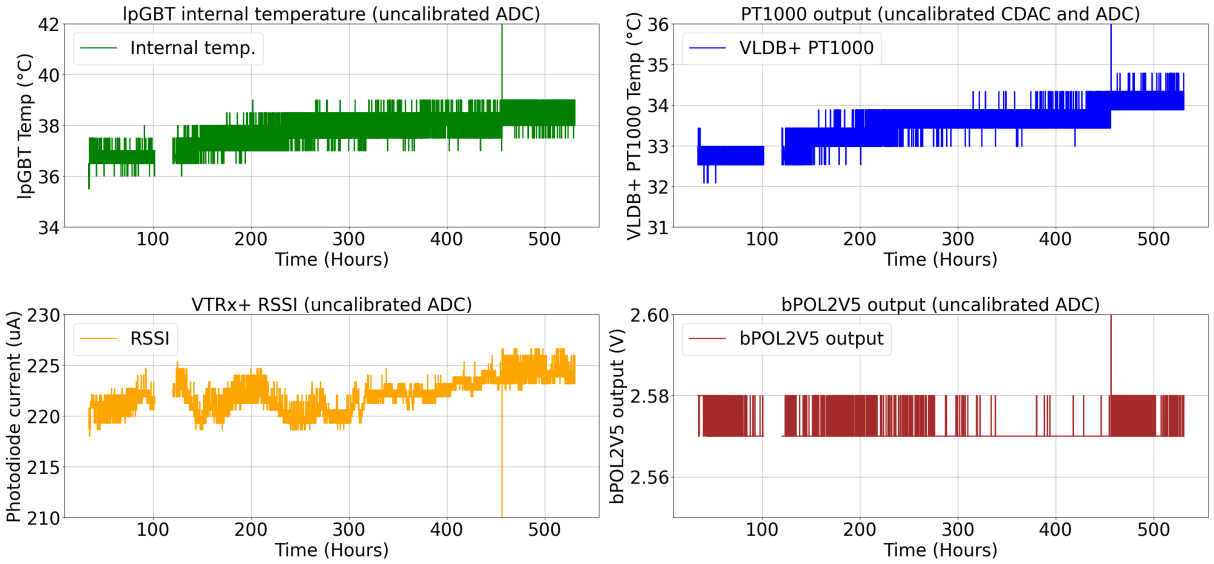

Figure 20: Performed lpGBT ADC readings during annealing

In Figure 20, the reading of the four ADCs during annealing is shown. Small drifts over time can be seen for the temperature readings and VTRx+ RSSI. A sudden change of the ADC readings at the hour 456 can be seen due to the lpGBT re-initialisation by which the VREF configuration was lost.

lpGBT status registers

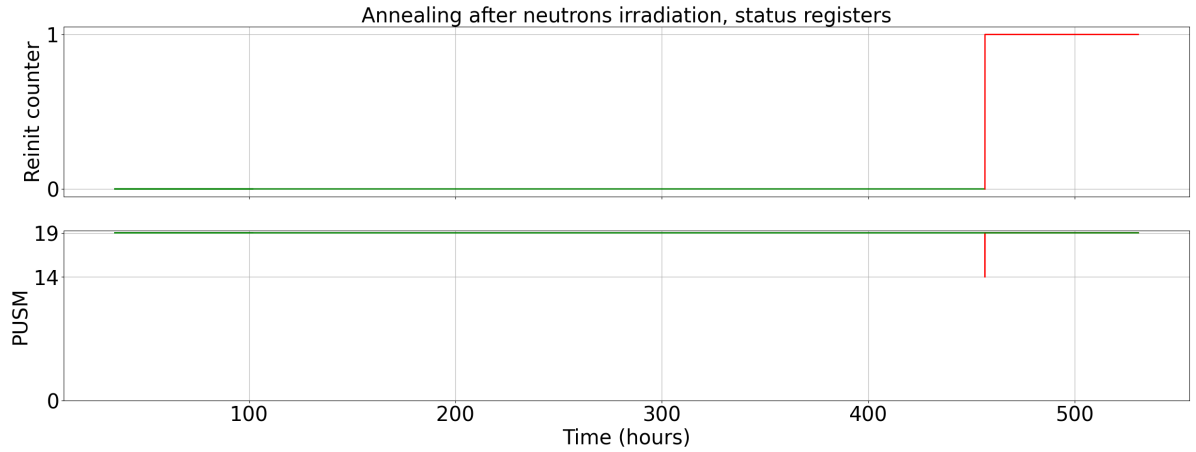

Figure 21: lpGBT and system status registers

During the annealing, there was a moment where the lpGBT power-up state machine jumped to PAUSE_FOR_DLL_CONFIG_DONE because of a Timeout and Watchdog trigger. Because of this, the system had to be reinitialised automatically by configuring the lpGBT and initialising the rest of the setup. The cause of the lpGBT reset is unknown. However, the lpGBT was able to properly operate just after this issue. The Figure 21 shows this event during the annealing.

lpGBT Downlink BERT

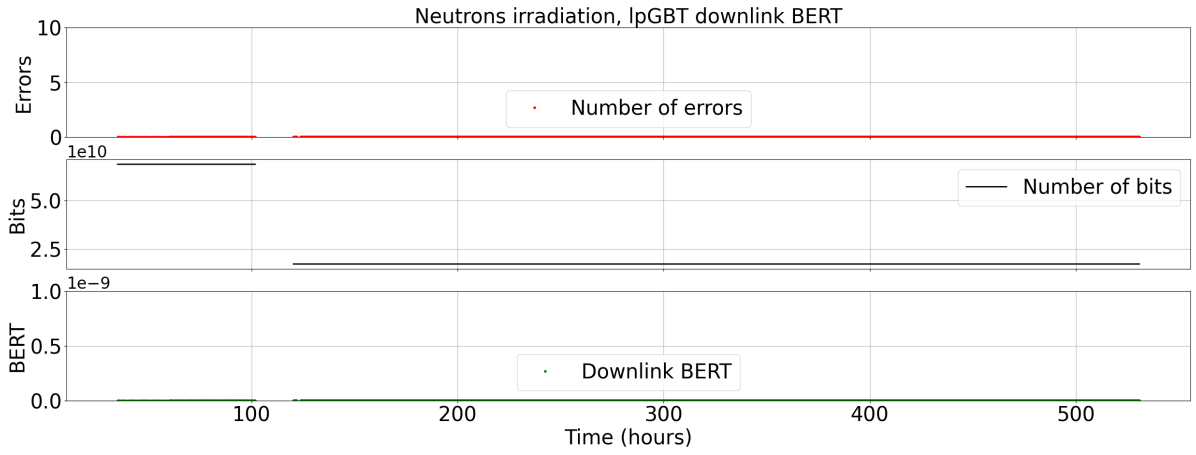

Figure 22: lpGBT Downlink BERT during annealing

During the annealing, no downlink errors were detected for every BERT cycle.

lpGBT Downlink FEC

During the annealing, the downlink FEC was most of the time zero. However, a few FEC were detected in some of the BERT cycles. It has been proven that these FEC were induced by an error in the software

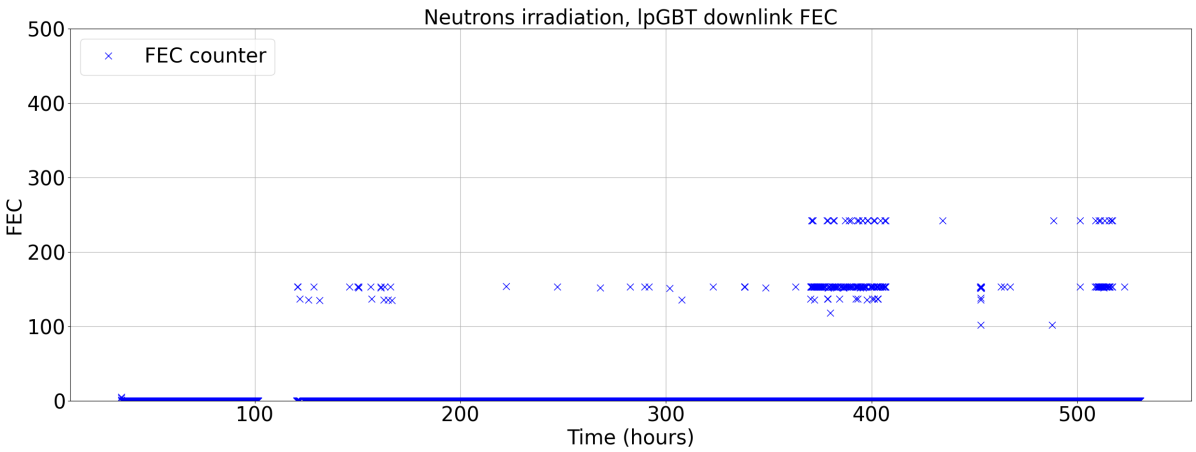

Figure 23: lpGBT Downlink FEC during annealing

explained in Section 7.

lpGBT Uplink BERT

During the annealing, no uplink errors were detected for every BERT cycle except for the specific moment where the lpGBT lost the Ready state.

lpGBT Uplink FEC

During the annealing, the uplink FEC remained at zero.

lpGBT and VTRx+ SEU

During the annealing, the SEU counters of both VTRx+ and lpGBT remained at zero.

7 Issues

During the irradiation campaign, several issues appeared that could be reproduced in the laboratory and were not related to the irradiation itself. This was due to an error in the software that was affecting the data taking of the system. Several tests were affected by it:

1. Downlink BERT was having many bunch of errors on every cycle. These were filtered before being plotted. A clear indicator that this was a fictitious problem was the stable Ready state of the lpGBT.
2. Downlink FEC was having in some cases different constant counter values. A clear indicator that this was a fictitious problem was that the FEC value was jumping backwards and forwards to the same specific value.
3. Uplink BERT was having the same behavior as Downlink BERT. However the results were also filtered to show up the real number of errors.
4. Uplink FEC was having the same behavior as Downlink FEC. The results were also properly filtered.

8 Conclusions

The VLDB+ was mainly designed to provide a board housing the lpGBT and VTRx+ devices to allow the users to get acquainted with these components. However, it also offers a wide range of possibilities like performing radiation tests of the full system by operating the lpGBT, VTRx+ and bPOL DC/DC converters at the same time. This is extremely valuable since it provides information of the compatibility of the four devices working together on a similar radiation environment.

The VLDB+ was irradiated with neutrons at the facilities of Louvain-La-Neuve. The lpGBT, VTRx+, bPOL12V and bPOL2V5 were irradiated during 35 hours and annealed during 500 hours. During the whole process, several tests were continuously executed to obtain data on how the devices were behaving while being irradiated and operating together.

The results show a good performance on all the irradiated devices. The lpGBT was operating during irradiation without any critical problem. Both downlink and uplink FEC were protecting the links against errors caused by the SEE. Due to the use of the lpGBT built-in test features, some anecdotal errors could be seen in the uplink direction. Moreover, the analog features also performed as expected. One unexplained issue was the wrong VTRx+ SEU readings using the lpGBT I2CMaster. However, this issue could be solved by an lpGBT reset which means that it could potentially be solved by performing an even simpler I2CMaster reset as well. Both lpGBT and VTRx+ SEU counters were showing good numbers exhibiting the protection of both devices against SEU.

The VTRx+ and bPOL DC/DC converters did not show any type of under-performance that could lead in a problematic behavior.

As a result of the performed radiations tests, the VLDB+ housing the lpGBT, VTRx+ and bPOL mezzanine worked properly.

References

[1] Bernier, Kim. Etude du comportement de détecteurs gazeux à micropistes MSGC sous irradiations intenses de neutrons rapides. Prom. : Grégoire, Ghislain